WHAT IS CLAIMED IS:

1. An apparatus comprising:

an interface; and

a cache coupled to the interface, wherein the cache is configured to transmit an address of a cache block to be evicted from the cache on the interface, and wherein the cache includes a memory configured to store a plurality of cache blocks including the cache block, and wherein the memory is coupled to receive the address from the interface, and wherein the memory is configured to access the cache block in response to the address for transmission on the interface.

2. The apparatus as recited in claim 1 wherein the cache is further configured to transmit the cache block on the interface.

3. The apparatus as recited in claim 1 wherein the cache includes an input path, and wherein a read address received from the interface traverses the input path to access the cache, and wherein the same input path is traversed by the address to access the cache block.

4. The apparatus as recited in claim 1 further comprising a tag memory coupled to receive a second address from the interface and configured to output a plurality of tags corresponding to cache storage locations eligible to store a second cache block addressed by the second address, wherein the cache is configured to select a first cache storage location of the cache storage locations to store the second cache block if the second address is a miss in the cache, and wherein the address of the cache block comprises a first tag of the plurality of tags, the first tag corresponding to the first cache storage location.

5. The apparatus as recited in claim 4 further comprising a plurality of comparators, each of the plurality of comparators coupled to receive a respective one of the plurality of tags and a tag portion of the second address, and wherein the plurality of comparators are configured to compare the plurality of tags to the tag portion of the second address to

detect the miss.

6. The apparatus as recited in claim 1 further comprising a data buffer coupled to the memory, wherein the data buffer is configured to store the cache block read from the memory for transmission on the interface.

7. The apparatus as recited in claim 1 wherein the interface is a bus.

8. The apparatus as recited in claim 1 wherein the cache transmits the address on the interface as a write transaction.

9. A cache comprising:

a memory configured to store a plurality of cache blocks; and

a control circuit configured to transmit an address of a cache block to be evicted from the cache on an interface to which the cache is couplable;

wherein the memory is coupled to receive the address from the interface and is configured to access the cache block in response to the address for transmission on the interface.

10. The cache as recited in claim 9 wherein the control circuit is configured to detect a miss in the cache and to select the cache block from the plurality of cache blocks in response to detecting the miss.

11. The cache as recited in claim 10 further comprising a tag memory coupled to receive a second address from the interface and configured to output a plurality of tags corresponding to cache storage locations eligible to store a second cache block addressed by the second address, wherein the control circuit is configured to select a first cache storage location of the cache storage locations to store the second cache block if the second address is a miss in the cache, and wherein the address of the cache block comprises a first tag of the plurality of tags, the first tag corresponding to the first cache storage location.

12. The cache as recited in claim 11 further comprising a plurality of comparators, each of the plurality of comparators coupled to receive a respective one of the plurality of tags

and a tag portion of the second address, and wherein the plurality of comparators are configured to compare the plurality of tags to the tag portion of the second address and are coupled to provide an indication of the comparison to the control circuit.

13. The cache as recited in claim 9 further comprising an input path for addresses received from the interface, wherein the same input path is used for the address of the cache block.

14. The cache as recited in claim 9 further comprising a data buffer coupled to the memory, wherein the data buffer is configured to store the cache block read from the memory for transmission on the interface.

15. The cache as recited in claim 9 wherein the address is part of a write transaction on the interface.

16. A method comprising:

a cache transmitting an address of a cache block to be evicted from the cache on an interface; and

in response to the transmitting, reading the cache block from a data memory of the cache for transmission on the interface.

17. The method as recited in claim 16 further comprising transmitting the cache block on the interface.

18. The method as recited in claim 16 further comprising:

detecting a miss of a second address in the cache; and

selecting the cache block for eviction responsive to the detecting.

19. The method as recited in claim 16 wherein the transmitting is part of a write transaction.

20. The method as recited in claim 16 further comprising storing the cache block in a data buffer responsive to the reading.